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Designing a low voltage amplifier through bulk driven technique with 0.6V supply voltage

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ABSTRACT: An ultra-low voltage rail-to-rail operational trans conductance amplifier (OTA) based on a standard digital 0.18µm CMOS process is described in this paper. Techniques for designing a 0.6 volt fully differential OTA are discussed including bias and reference current generator circuit. To rail-to-rail operation complementary input differential pairs are used where Bulk driven technique is used to reduce the threshold limitation of the MOSFET transistors. The OTA gain is increased by using auxiliary gain boosting amplifier and a inverting amplifier. The designed circuit was simulated by HSPICE software and 0.18 micrometer technology. This circuit is supplied with 0.6 v with a consume power of 30 microwatt and open loop gain voltage of 63 dB.

***Keywords*:** rail-to-rail, operational trans conductance amplifier, power consumption, low voltage supply, CMOS, HSPICE.

INTRODUCTION

The supply voltage of CMOS circuits should be low to facilitate transporting electronic devices like audio devices and also to reduce the size of VLSI circuits. However, the existence of limited threshold voltage in these transistors and that they cannot be reduced less than presents amounts in designing or making semiconductors prevents from reducing supply to a desirable amount. Different solutions are suggested for this problem. One of those solutions is the bulk-driven technique which a good technique in designing circuits with low supply voltage. To saturate transistors in this technique, the gate-source terminal should be biased first to create a strong inverse layer. Then, the input signal is applied to the bulk terminal of input transistors. Due the dependence of threshold voltage on bulk voltage, input voltage changes with the change of input voltage.

The bulk-driven technique was first introduces by Cuzinski et al. in 1987 as active components in an OTA differential input stage, later. It was then practices in 1991 and was used in some communicational circuits. Lots of articles are presented in this field so far(Haga and Hoseini, 2005; Rosenfeld and Kozak 2004; Bahmani and Fakhraie. 2000; Razavi, 2001; Tai, 2006).

One of the weaknesses of the bulk-driven technique is the low trans conductance of the source-bulk connection compared to the trans conductance of the gate-source connection (about 5 times more). Therefore, when the input differential pair of an amplifier is composed of bulk- driven transistors, the resulting DC gain is relatively low.

The highest voltage gain reached with this technique and 0.6 v supply voltage was equal to 70 dB with unit gain bandwidth of 100 kHz. (Giustolisi et al., 2003; Blalock and Allen, 1995) The results of the trans conductance amplifier with the supply voltage of 0.6 v, to reach voltage gain of 63 dB with 8.54 MHz unit gain bandwidth and a phase margin of 51 are explained in this article.

This paper is organized as following. the circuit performance is presented in first part. In section 3,the bias circuit and reference current generator are described. In section 4,the performance of the amplifier is summarized and some conclusions are offered in section 5.

Circuit Performance

Figure 1 shows the designed circuit (on micrometer scale). This circuit includes differential complementary pairs in input and its output branches are connected to a common gate amplifier; current sources were used as the load of this amplifier to increase the voltage gain. 4 auxiliary cascade amplifiers were used in the first stage and an inverter amplifier in the second stage to raise the gain from 22 dB in the main cascade circuit to 63 dB.

A compensator circuit(RC) was used to reach a margin phase of 51 degree. Weight and Length of figures 1 transistors Is show in table 1.

More Details

PMOS (M1 & M2) and NMOS (M 11 &12) differential pairs we used to reach rail to rail voltage performance in input in a way that the PMOS pair was active and the NMOS pair was cut-off with small amounts of common mode voltage but the NMOS pair was active and the PMOS pair was cut-off with large amounts of common mode voltage; both pairs are active with middle amounts.

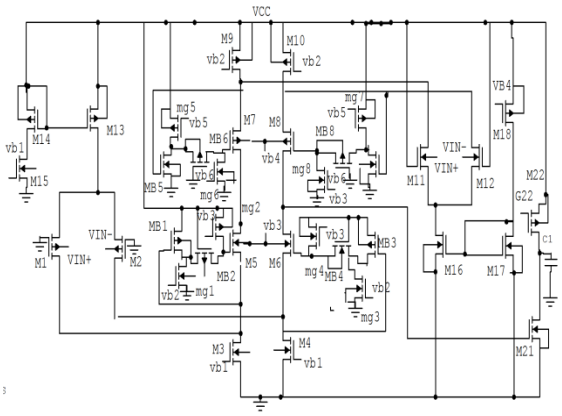


Figure 1. Proposed operational amplifier

To increase the CMRR of the circuit, M11, M14 and M15 are used as current source for input PMOS transistor pair and M16, M17 and M18 are used as current source for input NMOS transistor pair. Output branches of the PMOS input pair are applied to the common gate amplifiers (M5 & M6) that M7, M8, M9 and M10 are put as a load and as current sources for increasing the voltage gain of the amplifier.

M3 & M4 transistors are for input PMOS pair bias. Also, M7 & M8 are the amplifiers of the common gate and M3, M4, M5 and M6 transistors are as the load and M9 & M10 are for biasing input pairs.

Separate voltages were applied to the bulk terminal of these transistors to control the threshold voltage and increase the gain of M5, M6, M7 and M8 amplifiers.

AUXILIARY AMPLIFIERS

Mt1 and Mt2 transistors are second stage amplifiers to increase circuit gain for 14 dB. The auxiliary cascade amplifier (mb1, mb2, mb3, mb4, mb5, mb6, mb7 and mb8 transistors) are used to increase circuit gain.

Figure 2A shows one of the amplifiers when common gate transistors of the main circuit are connected to a constant voltage. Supposing the existence of resistance (r) in source, their output resistance will be

$$Rout \cong \frac{1.2 g_{m7}}{g_{ds7}} r \qquad (1)$$

if the auxiliary cascade circuit is added to the gate of these transistor (Fig:2B), the output resistance of transistors will be

$$Rout \cong \frac{1.2 \times g_{mb5} \times g_{mb6} \times g_{m7}}{g_{dsb5} \times g_{dsb6} \times g_{ds}} r \qquad (2)$$

Therefore, the total gain of the first stage will be increases due to the increase in the output resistance of common gate transistors.

Table 1. (A),(B) size of Figure 1. transistors

(A)		
M	L(μ)	W(μ)
M1,MB2	0.36	5
M3,M4	0.36	3.2
M5,M6	0.36	2.32
M7,M8	0.36	2
M9,M10	0.36	2.3
M11,M12	0.36	4
M13	0.36	7.9
M14,M15	0.36	5.5
M16	0.36	7
(B)		
M17,M18	0.36	5.1
MB1,MB3	0.36	1.7
MB2,MB4	0.36	3.62
MB5,MB7	0/36	0.7
MB6,MB8	0.36	1.6
MG1,MG3	0.36	1.7
MG2,MG4	0.36	0.7
MG5,MG7	0.36	1.5
MG6,MG8	0.36	2.3
M21, M22	0.36	0.7

With consider resistor of current source amount of output resistor equal will be

$$Rout \cong \frac{1.2 \times g_{mb5} \times g_{mb6} \times g_{m7}}{g_{dsb5} \times g_{ds1} \times g_{ds2} \times g_{dsb6} \times g_{ds7}} r \qquad (3)$$

R and C are selected as compensator circuits in a way to raise the phase margin of the circuit to about 51 degree.

CURRENT AND VOLTAGE SOURCES

One of the main goals in designing a current source and voltage resources is the independence of their amount form the supply voltage.

The shown circuit in figure 3 is a self-biased current source circuit which is sensitive to supply voltage. The amount of transistors, given the equality of source and gate voltage of MN3 & MN4 transistors, are selected in a way to provide output current of 1.5 μA in MN5 transistor.

Figure 4 shows a circuit which is used to generate independent voltage from supply source and also form the bias of transistors; the generation of bulk terminal voltage of amplifier transistors of the circuit are for increasing the gain.

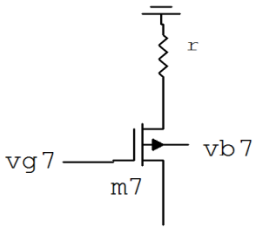


Figure 2. Simple common gate
A

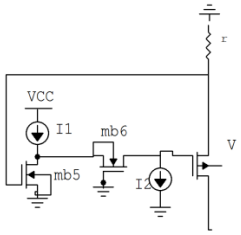
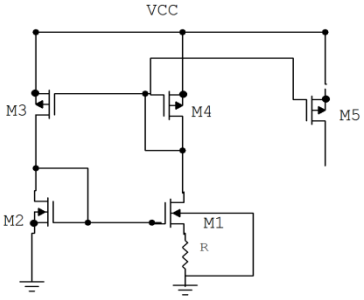


Figure 2. simple common gate with auxliary amplifier
B



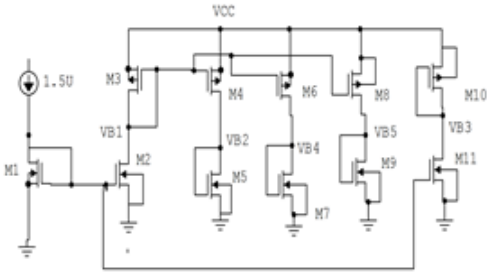


Figure 3. Low sensitivity reference current

Figure 4. Bias voltage generator circuit

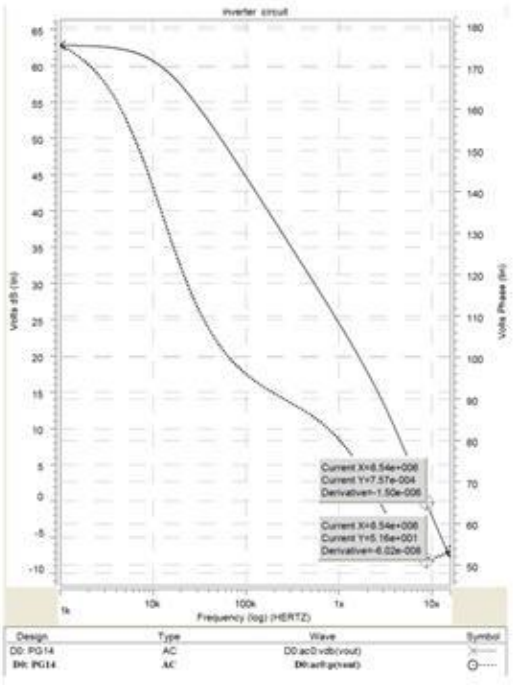


Figure 5. Open Loop Frequency Response Of Circuit

Table 2. (a) size of Figure 4 transistors,(b) size of Figure 3 transistors

M	L(µ)	W(µ)
M1	0.3	1
M2	0.36	0.4
M3	0.36	2.57
M4	0.4	2.29
M5	0.8	0.3
M6	0.4	4.4
M7	1	0.3
M8	0.4	2.34
M9	0.36	0.3
M10	0.3	0.7
M11	0.3	1

(a)

M	L(µ)	W(µ)
M1	0.36	1
M2	0.36	1
M3	0.36	2.57
M4	0.36	2.29
M5	0.36	0.3

(b)

Simulation Results

The gain and phase responses of the OTA, are shown in figure 5.The OTA has an open-loop DC gain of 63dB,a phase margin of 45 degree, and a unity-gain bandwidth of 90MHz, under a no load condition. For a capacitive load of 0.5 PF, phase margin increases to 51 degree while the unity-gain frequency reduce to 8.54MHz .The OTA operates from a 0.6 volt single power supply and consumes 30µW.

CONCULSION

The design of an ultra-low voltage, high performance folded cascade OTA circuit in a standard digital CMOS process is reported in this paper. To accommodate allow power supply voltage (0.6 volt), the bulk–driven MOSFET approach is used. The low gain disadvantage of the bulk-driven technique is circumvented by employing gain boosting amplifiers, permitting the achievement of a DC gain of 63 dB. Due to a lower body trans conductance, bulk-driven amplifiers inherently exhibit relatively poor gain. The primary conclusion of this paper is that bulk–driven amplifiers can be modified to operate with low power supply voltages while still exhibiting performance levels that satisfy the demands of state-of-the-art mixed-signal circuits.

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